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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,491	03/01/2004	Brian Moore	11157-073	7561

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EXAMINER	
NGUYEN, JIMMY	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,491	MOORE, BRIAN	
	Examiner	Art Unit	
	Jimmy Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34 - 47, 50, 54 - 57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34 - 47, 50, 54- 57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Argument

a. The amendment filed 1/27/05 has been carefully considered; however, upon further search the examiner makes a new ground of rejection

Claims Status

The examiner acknowledges the preliminary amendment filed 9/22/04 which indicated that claims 34 – 47, 50, 54 - 57 are pending.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 34 – 47, 50 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 19 of U.S. Patent No. 6,759,863. Although the conflicting claims are not identical, they are not

patentably distinct from each other because they are still in the same scope of the invention.

Matching Claims

10/788491	6, 759, 863
34	1
35	2
36	3
37	4
38	5
39	6
40	7
41	8
42	9
43	10
44	11
45	12
46	13
47	14
50	16

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to use a variable ring oscillator for the purpose of producing the different frequency during the testing process.

4. Claims 54 – 57 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 19 of U.S. Patent No. 6,759,863 in view of in view Pochmuller (US 6,535,,009)

As to claims 54 – 57, US patent # 6,759,863 claimed everything except for the test circuit is formed adjacent to a die containing the IC and formed on the dies near the edge of the wafer.

On the other hand, Pochmuller teaches the test circuit (7) is formed adjacent to a die containing the IC (2) and formed on the dies near the edge of the wafer (1).

It would have been obvious to one having an ordinary skill the art at the time of the invention was made to position the test circuit of Moore within the die area as disclosed in Pochmuller for the purpose of easy access between the test circuit and device under test.

DETAILED ACTION

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 34 – 47, 50, 54 – 57 are rejected under 35 U.S.C. 102(b) as being anticipated by Merrill et al (us 5,039,602).

As to claim 34, Merril et al disclose (fig 2) a test circuit (22) for testing an integrated circuit (86) on a wafer (84) the test circuit formed on the wafer with the integrate circuit, the test circuit comprising:

a) a base ring oscillator circuit (30)

b) a plurality of sub-circuits (32, 34) couple to the base ring oscillator circuit (30); and

c) a control circuit (32) to selectively couple the sub-circuits (34) to the base ring oscillator circuit (30) to produce different versions of a variable ring oscillator (30) circuit associated with a selected sub-circuit,

and wherein the test circuit (22) conducts a separate test of me integrate circuit (86) for at least one of the versions of the variable ring oscillator circuit (30)

As to claim 35, Merril et al disclose (fig 2) the test circuit of claim 34 wherein each test conducted by the test circuit is a parametric test (DC test).

As to claim 36, Merril et al disclose (fig 2) wherein the sub circuit (32, 34, 24) when couple: to the base ring oscillator circuit (30) change the frequency of oscillation of the variable ring oscillator circuit

As to claims 37, 38, 40, 41, Merril et al disclose (fig 2) the test circuit of claim 36 wherein at least one sub- circuit comprises a capacitive load (24) to change the frequency of oscillation of the variable ring oscillator circuit.

As to claim 44, Merril et al disclose (fig 2) the control circuit comprises a sequencer (32) to selectively couple the sub-circuits to the variable ring oscillator circuit to produce a series of test states.

As to claim 45, Merril et al disclose (fig 2) the test circuit (22) is formed on the wafer (84) with at least tow metallization layers of the IC (86).

As to claim 46, Merril et al disclose (fig 2) the test circuit (22) is formed on the wafer (84) with at least one metallization layers of the IC (86) and one polysilicon layer of the IC (86).

As to claim 47, Merril et al disclose (fig 2) the test circuit (22) produces a test result signal that is the output of the variable ring oscillator circuit (30).

As to claim 50, Merril et al disclose (fig 2) the control circuit further comprises a ring oscillator (30) adapted to provide a first clock signal, and a divider (32) coupled to the ring oscillator (30) and the sequencer and adapted to provide a second clock signal, wherein the second clock signal is provided to the sequencer so that the sequencer can

provide a series of test state signals to the variable ring oscillator circuit and plurality of sub-circuits.

As to claims 54, 55, Merril et al disclose (fig 2) the test circuit (22) is formed adjacent to a die containing the IC (86) and on the IC (86).

As to claims 56, 57, Merril et al disclose (fig 2) the test circuit (22) is formed on a large percentage of dies on the wafer (84) and near the edge of the wafer.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 39, 42, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill et al (us 5,039,602) in view of Lee (US 5,686,855).

As to claim 39, Merril et al disclose (fig 2) disclose everything except for the sub- circuit comprises a delay element to change the frequency of oscillation of the variable ring oscillator circuit.

On the other hand, Lee teaches the sub- circuit comprises a delay element (24, 28) to change the frequency of oscillation of the variable ring oscillator circuit.

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the teaching of Merrill et al with a delay circuit of Lee for the purpose of alternate the frequency of the signal during the testing process.

As to claims 42, 43, Lee disclose the delay element (24, 28) comprises at least one inverter is CMOS inverter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is 571-272-1965. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ramtez Nestor, can be reached on 571272 -2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
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JN.
August 8, 2005